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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,027	03/19/2001	Bharat Shivkumar	IR-1881	4072
2352	7590	01/27/2005	EXAMINER	
OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			MITCHELL, JAMES M	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/812,027

Applicant(s)

SHIVKUMAR ET AL.

Examiner

James M. Mitchell

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5,6,10-16 and 18-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,11 and 14 is/are allowed.
- 6) ☒ Claim(s) 2,3,5,6,10,12-16 and 18-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed November 4, 2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2 and 3, 5, 12, 13, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba (U.S. 6,071,755) in combination with Tamaki (U.S. 6,157,080).
4. Baba (Fig 20) discloses (cl. 2) an MCM device comprising a flat thin insulation substrate (34) having parallel top and bottom surfaces; a plurality of laterally displaced conductive vias (not labeled) extending between said top and bottom surfaces; a flip chip semiconductor die (31) having top and bottom surfaces; and an insulation cap (41, i.e. resin material) covering said die and covering the top surface of said substrate; (cl.5) and at least one passive component (53) which is beneath said insulation cap has at least one dimension (i.e. length) which is longer than its other dimensions (i.e. height), said passive component being connected to selected ones of said plurality of vias (i.e. contacting via) and being mounted on said first surface of said substrate with said at least one dimension disposed perpendicular to said first surface of said

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substrate with electrodes (not shown; i.e. in contact with item 32) on the bottom with its contact (32) on said die bottom surface; (cl. 3) along with and a second flip chip (31) semiconductor die having top and bottom surface and having at least an electrode (i.e. first electrode on bottom portion of chip) bottom surfaces with the electrode connected to respective ones of said plurality of vias; (cl. 13, 15, 16, 19) with solder balls (40) connected to the bottoms of said conductive via; (cl. 12) wherein the insulation cap has a peripheral, outer edge and therefore a rim surrounding an interior portion of said substrate, which receives the outer an outer peripheral edge of said substrate (i.e. top surface of substrate contact bottom portion of cap).

5. Baba does not appear to show at least second electrodes on said top surface or said second electrodes having contacts on said die bottom surface connected to respective ones of said plurality of vias.

6. Tamaki (Fig 7E) utilizes first and second electrodes (3,4) on said top and bottom surfaces and said first and second electrodes having contacts (8,6) on said die bottom surface connected to respective ones of said plurality of inherent vias (i.e. pads 7, 30 connected).

7. It would have been obvious to one of ordinary skill in the art to incorporate first electrodes on said top surface of the dies to be connected with contacts on said die bottom surface that is connected to respective ones of said plurality vias, in order to increase density without increasing height of the package as taught by Tamaki (Col. 15, Lines 36-44).

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8. Claims 6, 9, 10,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba et al. (U.S. 6,071,755) and Tamaki (U.S. 6,157,080) as applied to claims 2 and 5 and further in combination with Nakamichi (JP 410335544).

9. Neither Baba nor Tamaki appear to show said insulation cap with a plurality of spaced fins extending from a free surface thereof such that the passive component is between fins.

10. Nakamichi (Fig 1) utilizes an insulation cap (5) with a plurality of spaced fins (6,7) extending across the top outermost perimeter of an insulation cap/mold such that fins extend from a free surface thereof (i.e. outer perimeter of resin not in contact with anything, alternately area of cap beyond chip) and a component is between fins.

11 It would have been obvious to one of ordinary skill in the art to incorporate spaced fins in the insulation cap, such that fins extend from a free surface thereof, such that the passive component is disposed laterally between a respective pair of fins in order to provide high heat dissipation as taught by Nakamichi (English Abstract).

12. Claims 13 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba et al. (U.S. 6,071,755) and Tamaki (U.S. 6,157,080) in combination with Glenn (U.S. 6,586,667)

13. Baba and Tamaki disclose the elements stated in paragraphs 3-6 of this office action, but do not appear to show that the insulation cap's peripheral rim

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and outer peripheral edge of said substrate have cooperating projections and depressions to define a mold lock.

14. However Glenn utilize rims and substrate having cooperating projections and depressions to define a mold locks.

15. It would have been obvious to one of ordinary skill in the art to modify the cap and substrate of Baba to incorporate a cap with projecting member extending from its rim along with the substrate having depressions in order to enhance mold lock as taught by Glenn (Col. 9, Lines 8-19).

Response to Arguments

16. Applicant's arguments filed November 4, 2004 have been fully considered but they are not persuasive. Applicant contends that:

1) there are no vias in the wiring layer of Baba; 2) Baba fails to teach a perpendicular orientation of passive components or reorienting the passive component to a perpendicular position; 3) Nakamichi fails to disclose passive components between adjacent fin valleys, because its not mere rearrangement of parts, but critical and 4) that Glenn does not show molds lock with projections and depressions in the rim of the cap. Examiner respectfully disagrees.

17. In regards to argument no.: 1) even though Baba attempts to distinguish its "wiring layer" and vias, it does so in contrast to a single via that extends the full height of the substrate, in comparison to small holes that make up the wiring layer. Nevertheless an applicant may be its own lexicographer and the broad scope of the term via in the semiconductor art merely encompasses a hole that is subsequently filled/ plated with conductive material therein in part of a layer. see

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*e.g. USPTO classification index for class 257. As such, because Baba explicitly states that wiring layers are electrically connected by **holes** (Col. 11, Lines 12-30), which are subsequently filled with a conductive material, it is within the broad definition of a via;* 2) the vertical edges of the passive components are perpendicular to the horizontal surface of the substrate and there is no limitation that the passive component be oriented in a perpendicular position; 3) although applicant argues criticality in its placement of the passive component by indicating the "preferred" location, no such evidence exist. See MPEP 2164.08(c). Furthermore while Nakamichi does not explicitly disclose that heat fins included with passive components, it explicitly shows the use of fins with a semiconductor device, since Baba forms a semiconductor device, Nakamichi and Baba are in the same field of applicant's endeavor. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). As such there is motivation to incorporate fins for thermal dissipation of the device. In addition, because the broad scope of adjacent fins encompasses only that the fins are nearby, and two fins of a plurality of fins across the top of a package are adjacent and the passive component is laterally (from side-side of the component) between nearby/adjacent fins (e.g. fin to the left of component & fin to the right of component); 4) lastly, a pad that serves as a support that a chip is mounted on is within the scope of a substrate. The side surfaces of the pad/ substrate have depressions and a portion of the encapsulant within the groove is a projection, therefore it discloses the use of projections and depressions. While Glenn's process may be different than applicant's invention, the final product of a

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projection and depression for an interlock effect is disclosed in Glenn. In addition, once the encapsulant is hardened, the removal of the chip and pad/leads etc. results in a product having a cavity that is defined by a base and ring/rim portion.

Allowable Subject Matter

18. Claims 1, 11, and 14 are allowable.

The following is a statement of reasons for the indication of allowable subject matter: the prior art does not disclose or make obvious forming first and second electrodes on a top and bottom surface of a chip with a moldable conductive electrode extending over the top of a substrate, a uppermost surface of the die and in contact with vias including all the limitations of the independent claim,

Allowable Subject Matter

19. Claims 1, 11, and 14 are allowed. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose or make obvious a chip having electrodes on its top and bottom surfaces with a moldable conductive electrode [*wherein the electrode as indicated by applicant in its arguments filed April 24, 2003 forms an electrical connection consistent with the word electrode*] extending over an upper surface of the chip and substrate with the moldable conductive electrode further connected to vias extending in the substrate. Although heat sinks and encapsulants are known to be placed over chips and on a substrate and can be formed from a moldable conductive


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material, these materials are thermally conductive, but not electrically connected to a device element.


Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.



Jmm
January 21, 2005



CRAIG A. THOMPSON
PRIMARY EXAMINER